



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Masaharu Nagai et al. Art Unit : 1756
Serial No. : 10/694,986 Examiner : Daborah Chacko Davis
Filed : October 29, 2003 Confirmation No.: 5334
Title : METHOD FOR REMOVING RESIST PATTERN AND METHOD FOR
MANUFACTURING SEMICONDUCTOR DEVICE

MAIL STOP AMENDMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT

Applicants request consideration of the references listed on the attached PTO-1449 form. Under 37 C.F.R. § 1.98 (a)(2)(ii), only copies of foreign patent documents and/or non-patent literature are enclosed. Copies of any listed U.S. patents or U.S. patent application publications can be provided upon request.

This statement is being filed after a first Office action on the merits, but before receipt of a final Office action or a Notice of Allowance. A check for \$180 in payment of the late submission fee of §1.17(p) is enclosed. Please apply any other charges or credits to Deposit Account No. 06-1050.

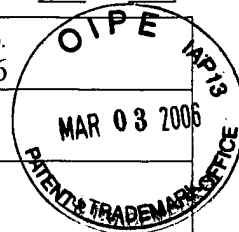
Respectfully submitted,

Date: March 3, 2006

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Substitute Form PTO-1449 (Modified)	U.S. Department of Commerce Patent and Trademark Office	Attorney's Docket No. 12732-171001	Application No. 10/694,986
Information Disclosure Statement by Applicant (Use several sheets if necessary) (37 CFR §1.98(b))		Applicant Masaharu Nagai et al.	
		Filing Date October 29, 2003	Group Art Unit 1756



U.S. Patent Documents

Examiner Initial	Desig. ID	Document Number	Publication Date	Patentee	Class	Subclass	Filing Date If Appropriate
	AA	2001/0052950	12-20-2001	Yamazaki et al.			03/16/2001
	AB	2002/0000551	01-03-2002	Yamazaki et al.			03/02/2001
	AC	2002/0127887	09-12-2002	Uehara et al.			05/11/2001
	AD	6,746,965	06-08-2004	Uehara et al.			07/30/2002
	AE	6,432,620	08-13-2002	Arao			08/16/2000
	AF	6,423,477	07-23-2002	Engelen et al.			10/07/1998
	AG	6,207,247	03-27-2001	Morita			03/26/1999
	AH	6,057,081	05-02-2000	Yunogami et al.			09/22/1997
	AI	5,506,168	04-09-1996	Morita et al.			10/11/1994
	AJ	4,692,205	09-08-1987	Sachdev et al.			01/31/1986
	AK	6,497,992	12/24/2002	Yunogami et al.			04/17/2000

Foreign Patent Documents or Published Foreign Patent Applications

Examiner Initial	Desig. ID	Document Number	Publication Date	Country or Patent Office	Class	Subclass	Translation	
							Yes	No
	AL							
	AM							
	AN							
	AO							
	AP							

Other Documents (include Author, Title, Date, and Place of Publication)

Examiner Initial	Desig. ID	Document
	AQ	Hatano et al., "A Novel Self-aligned Gate-overlapped LDD Poly-Si TFT with High Reliability and Performance", IEDM 97; Technical Digest of International Electron Devices Meeting, December 7, 1997, pp. 523-526.
	AR	Final Office Action dated December 06, 2005 for U.S. Serial No. 10/405,908 (Your Ref.: 12732-150001, Our Ref.: US6362)
	AS	
	AT	

Examiner Signature	Date Considered
EXAMINER: Initials citation considered. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.	